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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,623	CHAN, HUGO W.K.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 32-51 are presented for examination.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 32-51 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-29 of U.S. Patent No. 6,681,287. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference in language between the claimed present invention and the patented claimed invention relates to the special function being implemented in software. Using software for this purpose is an obvious type implementation and the only other type of implementation would be hard wired and as the specification is silent on being able to

implement the invention as a hard wired implementation, the software implementation is no more than an obvious addition to the claimed invention.

10/761,623	***6,681,287***
32. A smart memory integrated-circuit device, comprising:	1. A smart memory integrated-circuit device, comprising:
a memory array section;	a memory array section;
a special-function section *and special-function software used by the special-function section to* provide a function other than an exclusive memory function, wherein the special-function section and special-function software are packaged with the memory array section in a single smart memory integrated-circuit package;	a special-function section that provides a function other than an exclusive memory function and that is packaged with the memory array section in a single smart memory integrated-circuit package; and
wherein said single smart memory integrated-circuit package incorporates all memory functions of a standard memory that are provided by the memory array section *and special-function software* in addition to a special function that is provided by the special-function section in the single integrated-circuit package: and	wherein said single smart memory integrated-circuit package incorporates all memory functions of a standard memory that are provided by the memory array section in addition to a special function that is provided by the special-function section in the single integrated-circuit package: and
wherein the special-function section that provides a function other than an exclusive memory function is connected to the memory array section through a common internal bus within the smart memory integrated-circuit package to thereby significantly reduce the need for the memory array section to communicate with another external baseband integrated-circuit through an external common bus that has significantly greater propagation delay, parasitic capacitance, inductance, and resistance and that is required to be driven with higher current interface driving circuits.	wherein the special-function section that provides a function other than an exclusive memory function is connected to the memory array section through a common internal bus within the smart memory integrated-circuit package to thereby significantly reduce the need for the memory array section to communicate with another external, baseband integrated-circuit through an external common bus that has significantly greater propagation delay, parasitic capacitance, inductance, and resistance and that is required to be driven with higher current interface driving circuits.
Claim 33 is the same as:	Claim 2

Claim 34 is the same as:	Claim 3
Claim 35 is the same as:	Claim 4
Claim 36 is the same as:	Claim 5
Claim 37 is the same as:	Claim 6
Claim 38 is the same as:	Claim 7
Claim 39 is the same as:	Claim 8
Claim 40 is the same as:	Claim 9
Claim 41 is the same as:	Claim 10
Claim 42 is the same as:	Claim 11

43. A smart memory integrated-circuit device, comprising:

a memory array section:

a special-function section that provides a function other than an exclusive memory function *using software that is stored in the memory array section* and that is packaged with the memory array section in a single smart memory integrated-circuit package;

wherein said single smart memory integrated-circuit package incorporates all memory functions of a standard memory that are provided by the memory array section in addition to a special function that is provided by the special-function section in the single integrated-circuit package;

wherein the special-function section is connected to the memory array section through a common internal bus within the smart memory integrated-circuit package; and

wherein the single smart memory integrated-circuit package has substantially the

12. A smart memory integrated-circuit device, comprising:

a memory array section;

a special-function section that provides a function other than an exclusive memory function and

that is packaged with the memory array section in a single smart memory integrated-circuit package;

wherein said single smart memory integrated-circuit package incorporates all memory functions of a standard memory that are provided by the memory array section in addition to a special function that is provided by the special-function section in the single integrated-circuit package;

wherein the special-function section is connected to the memory array section through a common internal bus within the smart memory integrated-circuit package; and

wherein the single smart memory integrated-circuit package has substantially the

same type, fit, and form of a package for only a conventional memory package that has only the memory array section without the special function section.

44. A multi-media RAM (MMRAM) on a single integrated-circuit chip, comprising:

a memory array section that is formed on a single integrated-circuit die and that is contained in a multi-media RAM package;

a compressor/decompressor (CODEC) section integrally formed on the same single integrated-circuit die and contained in the same multi-media RAM package as the memory array section, said CODEC section formed on the same single integrated-circuit die with the same fabrication process as the memory array section; and

wherein the CODEC section is provided with a digital signal processor and CODEC software on the single integrated circuit die

wherein connections between the memory array section and the CODEC section are provided on the single integrated-circuit die.

Claim 45 is the same as:

46. The multi-media RAM of Claim 44 wherein the CODEC is provided as a digital signal processor a microcontroller *and CODEC software* on the single integrated-circuit chip.

same type, fit, and form of a package for only a conventional memory package that has only the memory array section without the special function section.

13. A multi-media RAM (MM RAM) on a single integrated-circuit chip, comprising:

a memory array section that is formed on a single integrated-circuit die and that is contained in a multi-media RAM package;

a compressor/decompressor (CODEC) section integrally formed on the same single integrated-circuit die and contained in the same multi-media RAM package as the memory array section, said CODEC section formed on the same single integrated-circuit die with the same fabrication process as the memory array section; and

wherein connections between the memory array section and the CODEC section are provided on the single integrated-circuit die.

14. wherein the CODEC section is provided as hardwired logic circuits on the single integrated-circuit die.

Claim 16

17. The multi-media RAM of claim 13 wherein the CODEC is provided with a digital signal processor on the single integrated circuit die.

18. The multi-media RAM of claim 17 wherein the CODEC is provided as a digital signal processor with a microcontroller on the single integrated-circuit chip.

Claim 47 is the same as:	Claim 19
Claim 48 is the same with the additional language as:	Claim 20
the CODEC section and the CODEC software	
49. The multi-media RAM of Claim 44 wherein the memory array section and the CODEC section are formed together monolithically as a single integrated circuit chip.	21. The multi-media RAM of claim 13 wherein the memory array section and the special-function section are formed together monolithically as a single integrated circuit chip.
Claim 50 is the same as with the additional language as:	Claim 22
software – line 8	
Claim 51 is the same as:	Claim 23

Claim Objections

5. Claim 44 is objected to as having 2 periods. Correction is required.

35 USC 112, 2nd paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 46 and are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

the phrase 'a digital signal processor a microcontroller' does not make sense; and,

claim 48 cannot depend on claim 13 as this claim was cancelled.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (703) 305-9706. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (703) 308-1756. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center receptionist whose telephone number is (703) 305-3800/4700.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

September 7, 2004